ABSTRACT OF THE DISCLOSURE

A processor changes the mapping of register addresses to registers dependent on an instruction field. In one particular embodiment, the mapping may be changed for byte addressing of the registers. A register mapping in which each register address maps to either the least significant byte or the next least significant byte of a subset of the registers may be supported, as well as a register mapping in which each register address maps to the least significant byte of each register, in one implementation. In one particular implementation, the instruction field may be a prefix field (e.g. a prefix byte). The processor may provide for uniform addressing of registers (e.g. byte addressing of the registers) responsive to a prefix field, in other embodiments, irrespective of the addressing provided if the prefix field is not included, or is encoded differently than the encoding which results in the uniform addressing.